IN THE SPECIFICATION:

Please replace paragraph number **[0004]** with the following rewritten paragraph:

[0004] Another type of memory device is a programmable read only memory (PROM) device. Unlike ROM devices, PROM devices are programmable after their design and fabrication. To render them programmable, PROM devices are typically provided with an electrical connection in the form of a fusible link (fuse). There are a considerable number of fuse designs used in PROM devices, such as those disclosed in IEEE Transactions on Electron Devices, Vol. 33, No. 2, p.~~250-~~ 250-253 (Feb. 1986), and in U.S. Patent Nos. 5,589,706, 4,491,860, 5,625,218, 4,796,075, and 4,740,485, the disclosures of which are incorporated herein by reference. Perhaps the most common fuse design is a metal or polysilicon layer which is narrowed or "necked down" in one region. To blow the fuse, a relatively high electrical current is driven though the metal or polysilicon layer. The current heats the metal or polysilicon above its melting point, thereby breaking the conductive link and making the metal layer or polysilicon discontinuous. Usually, the conductive link breaks in the narrowed region because the current density (and temperature) is highest in that region. The PROM device is thus programmed to conducting and non-conducting patterns, thereby forming the 1 or 0 comprising the data stored in the memory device.

Please replace paragraph number **[0022]** with the following rewritten paragraph:

[0022] Next, polysilicon layer 14 is formed over dielectric layer 12 and field isolation regions 10. Polysilicon layer 14 may be formed by any suitable deposition method known in the art, such as physical or chemical vapor deposition. Preferably, polysilicon layer 14 is deposited by ~~low-~~low-pressure CVD to a thickness ranging from about 800 to about 2000 angstroms. Polysilicon layer 14 is then doped, preferably with an n-type dopant such as phosphorous, by any suitable ion implantation or doping process known in the art. Alternatively, polysilicon layer 14 can be *in-situ* doped during deposition of polysilicon layer 14 by including a gas containing the desired dopant in the deposition atmosphere.

Please replace paragraph number **[0023]** with the following rewritten paragraph:

[0023] Next, conductive layer 16 is formed over polysilicon layer 14 by any suitable process known in the art. Conductive layer 16 may comprise any conductive material that has a lower resistance and/or a lower melting point than polysilicon layer 14, such as titanium silicide, polycide, or tungsten silicide. Preferably, tungsten silicide is employed as conductive layer 16. When tungsten silicide is employed as conductive layer 16, the tungsten silicide layer may be formed by any process yielding the desired physical and chemical characteristics, such as CVD or ~~co~~ co-sputtering. Preferably, this tungsten silicide layer is formed by CVD using tungsten hexafluoride (WF_6) and silane (SH_4) at a temperature ranging from about 400 to about 500°C. until a thickness of about 600 to about 1500 angstroms is obtained.

Please replace paragraph number **[0026]** with the following rewritten paragraph:

[0026] Referring to Figure 5, a layer comprising titanium (Ti) (hereafter the "~~T~~Ti layer") is then deposited or otherwise formed over substrate 2, isolation regions 10, and gate structure 20. The Ti layer may be formed by any process imparting the desired physical and chemical characteristics to the layer. Preferably, the Ti layer is formed by a sputter deposition process, such as sputter deposition using a Ti target in a vacuum containing argon, to a thickness ranging from about 200 to about 500 Å, and more preferably 300 Å. The Ti layer may be a titanium compound or titanium alloy since the layer need not be, but preferably is, substantially pure titanium. For example, alloying elements or other metals may be introduced into the Ti layer to provide better physical and chemical properties.

Please replace paragraph number **[0027]** with the following rewritten paragraph:

[0027] The Ti layer is then converted to a layer comprising titanium and nitrogen, such as Ti_xN_y where x can range from more than 0 to less than 1.0 {hereafter "titanium nitride (or TiN) layer 24"}. In one embodiment, this conversion is performed by annealing the Ti layer in a ~~nitrogen~~ nitrogen-containing atmosphere for a time and temperature sufficient to convert the

titanium to a mixture of titanium and nitrogen. In this annealing process, the temperature may range from about 600 to about 750°C., and is preferably about 650°C., and the time may range from about 20 to about 120 seconds, and is preferably about 60 seconds. The nitrogen-containing atmosphere of the annealing process may comprise a gas or a mixture of gases containing nitrogen, such as nitrogen, ammonia, or mixtures thereof. The annealing atmosphere may also contain other gases, such as argon or hydrogen. Preferably, the nitrogen-containing atmosphere contains substantially pure nitrogen gas.

IN THE CLAIMS:

Claims 10, 27, 30, 34, and 36 have been amended herein. All of the pending claims 1 through 37 are presented below. This listing of claims will replace all prior versions and listings in the application. Please enter these claims as amended.

1. (Original) A semiconductor circuit fuse, comprising:
an insulating substrate;
a refractory metal nitride layer disposed above the insulating substrate; and
a tungsten silicide layer disposed over the refractory metal nitride layer.

2. (Original) The semiconductor circuit fuse of claim 1, wherein the insulating substrate is an isolation region.

3. (Original) The semiconductor circuit fuse of claim 2, wherein the isolation region is a field oxide region.

4. (Original) The semiconductor circuit fuse of claim 3, wherein the field oxide region is disposed on a semiconductor substrate.

5. (Original) The semiconductor circuit fuse of claim 4, wherein the semiconductor substrate is a silicon wafer.

6. (Original) The semiconductor circuit fuse of claim 1, wherein the refractory metal nitride layer and the tungsten silicide layer are configured to a similar shape.

7. (Original) The semiconductor circuit fuse of claim 6, wherein the similar shape comprises a neck portion located between terminal portions.

8. (Original) The semiconductor circuit fuse of claim 7, wherein the neck portion is smaller in width than the terminal portions.

9. (Original) The semiconductor circuit fuse of claim 8, wherein the neck portion has a width within a range of about 0.2 to about 1 micron.

10. (Currently Amended) The semiconductor circuit fuse of claim 9, wherein the width of the neck portion is about 0.35 ~~microns~~micron.

11. (Original) The semiconductor circuit fuse of claim 9, wherein a length of the neck portion is within a range of about 1 to about 10 microns.

12. (Original) The semiconductor circuit fuse of claim 11, wherein the length of the neck portion is about 3.5 microns.

13. (Original) The semiconductor circuit fuse of claim 1, wherein the refractory metal nitride layer comprises titanium nitride.

14. (Original) A semiconductor circuit fuse, comprising:
an insulating substrate;
a refractory metal nitride layer disposed above the insulating substrate; and
a conductive layer disposed over the refractory metal nitride layer.

15. (Original) The semiconductor circuit fuse of claim 14, wherein the insulating substrate is an isolation region.

16. (Original) The semiconductor circuit fuse of claim 15, wherein the isolation region is a field oxide region.

17. (Original) The semiconductor circuit fuse of claim 16, wherein the field oxide region is disposed on a semiconductor substrate.

18. (Original) The semiconductor circuit fuse of claim 17, wherein the semiconductor substrate is a silicon wafer.

19. (Original) The semiconductor circuit fuse of claim 14, wherein the refractory metal nitride layer includes titanium.

20. (Original) The semiconductor circuit fuse of claim 14, wherein the refractory metal nitride layer comprises titanium nitride.

21. (Original) The semiconductor circuit fuse of claim 14, wherein the conductive layer is selected from the group consisting of a metal, metal alloy and metal compound.

22. (Original) The semiconductor circuit fuse of claim 14, wherein the conductive layer comprises tungsten silicide.

23. (Original) The semiconductor circuit fuse of claim 14, including configuring the refractory metal nitride layer and the conductive layer to a similar shape.

24. (Original) The semiconductor circuit fuse of claim 23, wherein the similar shape comprises a neck portion located between terminal portions.

25. (Original) The semiconductor circuit fuse of claim 24, wherein the neck portion is smaller in width than the terminal portions.

26. (Original) The semiconductor circuit fuse of claim 25, wherein the neck portion has a width within a range of about 0.2 to about 1 micron.

27. (Currently Amended) The semiconductor circuit fuse of claim 26, wherein the width of the neck portion is about 0.35 ~~microns~~micron.

28. (Original) The semiconductor circuit fuse of claim 27, wherein a length of the neck portion is within a range of about 1 to about 10 microns.

29. (Original) The semiconductor circuit fuse of claim 28, wherein the length of the neck portion is about 3.5 microns.

30. (Currently Amended) A method of using a fuse in an integrated circuit, comprising:

providing a fuse containing a conductive layer and a refractory metal nitride layer disposed above an insulating substrate and having a neck portion extending between terminal portions, the neck portion having a width of about 0.35 ~~microns~~micron; and

applying electrical current between the terminal portions sufficient to blow the fuse by causing the neck portion of the ~~conductive layer~~ fuse to melt.

31. (Original) The method of claim 30, including providing the neck portion with a length of about 3.5 microns.

32. (Original) The method of claim 30, including applying an electrical current within a range of about 1 to about 25 mA.

33. (Original) The method of claim 30, including applying an electrical current of about 5.5 mA.

34. (Currently Amended) A method of using a fuse in an integrated circuit, comprising:

providing a fuse containing a conductive layer and a refractory metal nitride layer disposed above an insulating substrate and having a neck portion extending between terminal portions; and

applying electrical current within a range of about 1 to about 25 mA between the terminal portions sufficient to blow the fuse by causing the neck portion of the ~~conductive layer~~ fuse to melt.

35. (Original) The method of claim 34, including providing the neck portion with a length of about 3.5 microns.

36. (Currently Amended) The method of claim 34, including providing the neck portion with a length of about 0.35 ~~microns~~micron.

37. (Original) The method of claim 34, including applying an electrical current of about 5.5 mA.

REMARKS

No new matter has been added. The amendments to the claims address typographical and spelling errors, and improve antecedent basis. The amendments do not affect, or surrender, any scope of any claim as originally filed.

The Applicants again request entry of the amendments as set forth herein prior to examination of the application on the merits.

Respectfully submitted,

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